UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/294,341	04/20/1999	MASAAKI HIROKI	0756-1964	6027

31780 7590 04/19/2005

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/294,341	HIROKI, MASAAKI	
	Examiner	Art Unit	
	Regina Liang	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-17,19-23,25-35 and 37-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-17,19-23,25-35 and 37-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

2. Claims 1, 3-6, 8-10, 12, 14-17, 19, 21-23, 25, 27-31, 33-35, 37, 39-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al (US. PAT. NO. 6,229,513 hereinafter Nakano) in view of Okada et al (US. PAT. NO. 5,734,378 hereinafter Okada).

As to claim 1, Fig. 1 of Nakano discloses a display device comprising a display panel having a TFT (switching element), a scanning line driving circuit (gate drivers 140), a signal line driving circuit (drain driving 130), a control circuit (110) and a video signal processing circuit (100). Nakano also disclose the control circuit (110) generating a first clock signal D4 (first signal) and a second clock signal D5 (second signal) having a different phase from the first clock signal D4 (first signal), and the clock signal D4 is transmitted to a group A of drain drivers 130 and the second clock signal D5 is transmitted to a group B of drain driver 130 (Fig. 4B and col. 6, lines 23-37 for example); this corresponds to the first signal is input to at least one of the signal line driving circuit and the scanning line driving circuit and the second signal is input to at least one of the signal line driving circuit and the scanning line driving circuit.

Nakano differs from the claim in that the control circuit does not have a delay circuit for producing the phase difference in the second signal (second clock signal) with respect to the phase of the first signal (first clock signal). However, Figs. 2 and 3 of Okada teaches a control circuit of a display device having a delay circuit (40 in Fig. 2) for producing a phase difference (ϕ) in a second signal (CK') with respect to a phase of a first signal (CK). Thus it would have

been obvious to one of ordinary skill in the art at the time the invention was made to modify the control circuit of Nakano to have a delay circuit for producing a second clock signal having a different phase from the first clock signal as taught by Okada since the high-speed data transfer and sampling can be easily performed (col. 10, lines 25-26 of Okada).

As to claim 3, Nakano teaches the first signal and the second signal are clock signals.

As to claims 4, Fig. 4B of Nakano shows that the first clock signal (D4) has a different rise time period and a different signal fall time period from the second clock signal (D5).

As to claims 5, Fig. 3 of Okada also teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claim 6, Fig. 4B of Nakano shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claims 8, note the discussion of claim 1 above. In addition, Nakano teaches each of the first signal and the second signal is a clock signal. Fig. 3 of Okada shows a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claims 9 and 45, Fig. 4B of Nakano shows the first clock signal (D4) has a reversed phase relation with the second clock signal (D5).

As to claim 10, Fig. 4B of Nakano shows that the first clock signal (D4) has a different rise time period and a different signal fall time period from the second clock signal (D5).

As to claim 12, Fig. 3 of Okada also teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal

As to claims 14 and 21, note the discussion of claim 8 above. In addition, Nakano discloses the first clock signal D4 (first signal) and the second clock signal D5 are input to a same shift register circuit or a same latch circuit as claimed (153 or 154 in Fig. 7, and see col. 9, line 61 to col. 10, line 4 for example).

As to claims 15 and 22, Fig. 4B of Nakano shows the first clock signal (D4) has a reversed phase relation with the second clock signal (D5).

As to claim 16, Nakano teaches the first signal and the second signal are clock signals.

As to claims 17 and 23, Fig. 4B of Nakano shows that the first clock signal (D4) has a different rise time period and a different signal fall time period from the second clock signal (D5).

As to claims 19 and 25, Fig. 4B of Nakano shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

Claims 27 and 33, which are method claims corresponding to the above apparatus claims 1 and 8 are rejected for the same reasons as stated above since such method "steps" are clearly read on by the corresponding "means".

As to claims 28, Nakano teaches the first signal and the second signal are clock signals.

As to claims 29 and 35, Fig. 4B of Nakano shows that the first clock signal (D4) has a different rise time period and a different signal fall time period from the second clock signal (D5).

As to claim 30 and 37, Fig. 3 of Okada also teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal

As to claims 31, Fig. 4B of Nakano shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claim 34, Fig. 4B of Nakano shows the first clock signal (D4) has a reversed phase relation with the second clock signal (D5).

As to claims 39-44, Nakano as modified by Okada discloses the claimed invention except for a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time period of the first signal, and shorter than a half of a signal holding time period. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the display device of Nakano as modified by Okada to have the length of the phase difference as claimed, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claims 7, 13, 20, 26, 32, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano and Okada as applied to claims 1, 8, 14, 21, 27 and 33 above, and further in view of Shimada (US. PAT. NO. 5,801,678 hereinafter Shimada).

Nakano as modified by Okada teaches the display device including a transmission type LCD panel. Nakano as modified by Okadata does not disclose the display device is a projection type display device. However, Fig. 2 of Shimada teaches a LCD display device is a projection

type display device having a light source (202) for projection. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Nakano as modified by Okada to be a projection type display device as taught by Shimada so as to provide a projection type LCD device for projecting the images on the projection screen.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-10, 12-17, 19-23, 25-35, 37-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Go (US. PAT. NO. 6,320,566) teaches a driving circuit for LCD in dot inversion method.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

4/12/05